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Research Article

Design and Simulation of High-Efficiency 0.18µm CMOS AC-DC Converter with Multi-Output Low-Dropout (LDO) Voltage Regulator for Energy Harvesting Applications

*Hawraa Abdul-Elah Kadhum

Assistant Lecturer, Al-Muthanna University, Muthanna- Iraq.

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***Corresponding Author: Hawraa Abdul-Elah Kadhum**
Assistant Lecturer, Al-Muthanna University, Muthanna- Iraq.
ORCID: 0009-0008-5063-8033

Abstract

Low-power energy harvesting has emerged as a critical technology for self-powered wireless sensor nodes, biomedical implants, RFID tags, and wearable electronic systems. However, ambient micro-generators, such as piezoelectric, thermoelectric, and electromagnetic transducers, typically produce irregular low-amplitude alternating current (AC) voltages that require high-efficiency rectification and precise voltage regulation. Traditional diode and bipolar junction transistor (BJT) bridge rectifiers suffer from excessive forward voltage drops (0.7 V – 1.4 V) and high substrate leakage currents, severely degrading power conversion efficiency (PCE). This paper contains full integrated & low voltage & high-efficiency AC-DC converter coupled with a multi-output Low Drop out (LDO) voltage regulator designed with standard 0.18µm CMOS technology & validated via HSPICE simulations. The proposed full-bridge CMOS rectifier operates at 1.0 Vpk input (100 Hz) and achieves a power conversion efficiency of 96% with an ultra-low output voltage drop of only 40 mV (a 33% reduction compared to baseline literature), and a quiescent power consumption of 250 nW. To deliver stable supply rails for heterogeneous system-on-chip (SoC) domains, an all-MOS LDO regulator is designed to accept wide input voltages range between 2.5 V and 6.0 V and supply three digitally selectable regulated output (1.0 V and 1.2 V, and 1.8 V). The LDO incorporates a temperature-compensated PMOS differential error amplifier, a 2.1 V Zener-based reference generator with a tri-mode NMOS switch network, and an integrated overcurrent shield circuit. Simulation results demonstrate a load-regulation of 1200 µV/mA (a 2.9 × performance gain over existing work) and a line-regulation of 27 mV/V (1.76 × improvement), with a power supply rejection ratio (PSRR) of -31.4 dB. The proposed integrated power management solution offers superior efficiency, wide input compliance, and robust short-circuit protection for next-generation self-powered electronic systems.

Keywords: *CMOS Rectifier, AC-DC Converter, Energy Harvesting, Low-Dropout (LDO) Regulator, Multi-Output Voltage Regulation, Overcurrent Protection, HSPICE, Power Conversion Efficiency (PCE).*

1. Introduction and Background:

With the growing number of devices being connected to Internet of Things (IoT), wearable health monitors, wireless sensor networks (WSN), the need for energy sources that are miniaturized and self-powered is increasing. Traditional battery-based technologies are limited in their ability to provide power for a prolonged period, often needing maintenance, replacement or recharging. An alternative method for extending the operational autonomy is ambient energy harvesting, which involves harvesting energy from the ambient kinetic, mechanical vibration, solar or thermal energy.

But ambient energy transducers produce small voltage AC output signals, which typically have amplitudes of 1.0 V or less and are at sub-kilohertz frequencies. These raw AC voltages are not directly usable with integrated circuits: the signal has to be rectified to become an unregulated DC voltage and then stabilized using a precision voltage regulator.

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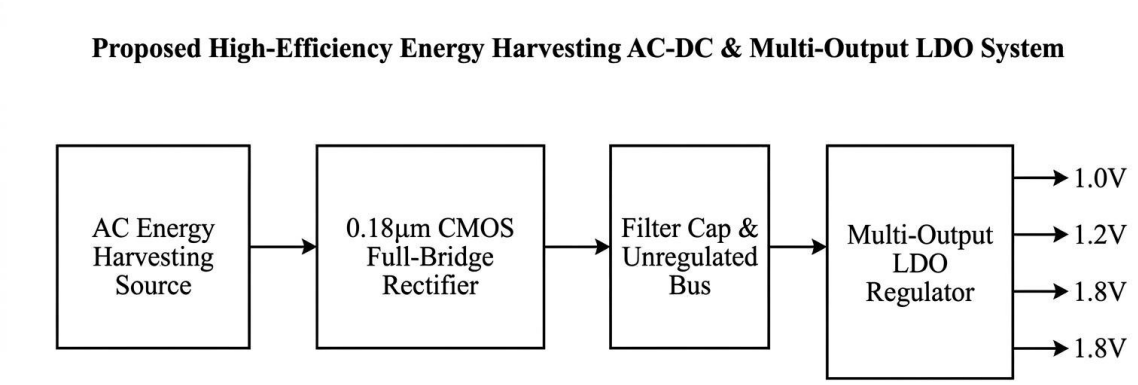

Figure 1: High-Efficiency Energy Harvesting System Architecture showing the AC source, 0.18µm CMOS Full-Bridge Rectifier, and Multi-Output LDO Regulator.

1.1 Comparative Analysis of Rectifier Topologies:

Converting micro-scale AC signals to DC requires minimal conduction loss. Standard PN-junction diode bridge rectifiers introduce significant forward voltage drops (2VD ≈ 1.2 V − 1.4 V), rendering them completely inactive at 1.0 V peak inputs. Bipolar Junction Transistor (BJT) rectifiers reduce conduction resistance but suffer from severe substrate leakage currents (Isub) due to collector-base junction parasitics at elevated frequencies.

MOSFET-based full-bridge rectifiers in standard CMOS technology overcome these bottlenecks by replacing passive diodes with low-on-resistance MOS switches (RDS (on)). By eliminating threshold voltage drops, CMOS active rectifiers achieve high power efficiency while maintaining full compatibility with low-cost planar silicon processes.

Rectifier Topology	Voltage Drop (ΔV)	Power Dissipation / Efficiency	Substrate Leakage & Area	Process Integration
PN Diode Bridge	High (1.2 V – 1.4 V)	Very High Loss / Low PCE	Negligible / Large Off-Chip Area	Non-Standard Option
BJT Transistor Bridge	Moderate (0.4 V – 0.7 V)	High Leakage Loss	High Isub Parasitics / Large Area	Complex BiCMOS
Active CMOS Bridge (Proposed)	Ultra-Low (40 mV)	Minimal Loss (250 nW) / PCE=96%	Controlled / 4% Area of Diode	Standard 0.18µm CMOS

1.2 The Critical Role of Low-Dropout (LDO) Voltage Regulators:

A converter that converts an (AC) to (DC) will produce output voltage ripple and will dynamically change in response to fluctuation in ambient kinetic input or load demand. Linear regulators are used in microprocessors, digital logic and wireless transceivers to ensure reliable performance, and are referred to as low-dropout (LDO) regulators. Unlike switching regulators, which require bulky physical inductors that induce electromagnetic interference (EMI), LDO regulators provide ripple-free DC rails with low quiescent currents and small silicon footprints.

2. Proposed System Architecture & Circuit Design:

The integrated power management circuit concept consists of two blocks, the active CMOS full-bridge rectifier and the multi-output LDO voltage regulator.

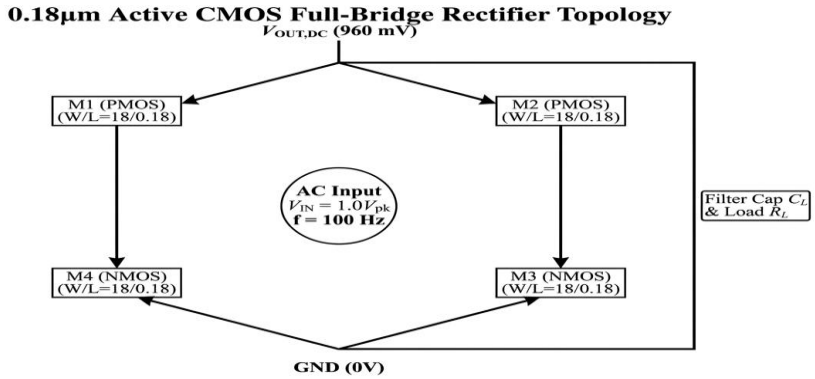

Figure 2: Active 0.18µm CMOS Full-Bridge Rectifier Circuit Schematic featuring cross-coupled PMOS switches (M1, M2) and NMOS switches (M3, M4).

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2.1 Active CMOS Full-Bridge Rectifier Topology:

Its ac-DC converter is combination of three cross coupled MOSFET, two PMOS switches (M1, M2) and two NMOS switches (M3, M4). To reducing the channel resistance & suppress the parasitic capacitor between gate and drain of all four transistors, the aspect ratios of the transistors are set to be W/L = 18µm / 0.18µm.

When the input voltage (VAC) is positive (VAC>0), strong inversion occurs in transistors M1 and M4, allowing current to flow through load RL to ground. In turn, when the voltage across M2 and M3 are negative (VAC < 0), M2&M3 are conducting whereas M1 and M4 are cut off.

2.2 Mathematical Model of Rectifier Efficiency and Voltage Drop:

The total voltage drops across the active bridge (ΔVrect) is governed by the channel resistance of the conducting PMOS and NMOS pair:

$$\Delta Vrect = I load \cdot (RDS(on), P + RDS(on), N)$$

Where $RDS(on) = L / [\mu \cdot Cox \cdot W \cdot (VGS - Vth)]$. By selecting minimum channel length $L = 0.18\mu m$ and transistor width $W = 18\mu m$, the internal voltage drop is constrained to just 40 mV at a peak load current of 950 μA.

The (PCE) is defined as the ratio of average DC O/P power (PDC) to total AC I/P power (PAC, in):

$$PCE = \left[PDC — PAC, in\right] \times 100\%$$

$$= [(VOUT, DC \cdot IOUT, DC) / ((1/T) \int 0\text{^}T\ vin(t) \cdot I\ in(t)\ dt)] \times 100\%$$

With an input amplitude of 1.0 Vpk, the proposed rectifier yields $VOUT, DC = 960\ mV$, delivering a $PCE\ of$ 96.0% with a static power consumption of only 250 nW.

Multi-Output CMOS LDO Regulator Topology with Overcurrent Shield

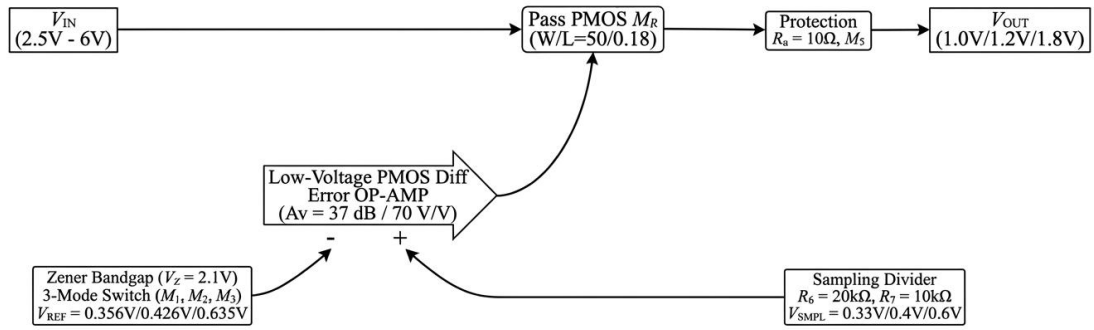

Figure 3: Complete Multi-Output CMOS LDO Regulator Circuit Schematic showing PMOS Error Amplifier, Zener Reference, NMOS Selector Network, and Overcurrent Protection.

2.3 Proposed Multi-Output Low-Dropout (LDO) Voltage Regulator:

The rectifier output is coupled with the multi-output LDO regulator that works on an I/Prange from (2.5 V) to (6.0 V). The regulator features a PMOS pass transistor (MR, W/L = 50µm / 0.18µm), low voltage high gain differential error amplifier, a stable 2.1 V Zener reference, a digitally controlled reference switch network, a resistive sampling bridge (R6, R7), and an overcurrent protection loop (R8, M5).

2.4 High-Gain PMOS Differential Error Amplifier Design:

To enable low-voltage operation and maximize common-mode input range, the I/P stage of the error amplifier utilizes a(PMOS) differential pair (M1, M2). An active tail current mirror (M5, M6) supplies a constant bias current Itail ≈ 600 µA. Degeneration resistors R1, R2 = 500 Ω and active load resistors R3, R4 = 1.12 kΩ enhance internal impedance and stabilize amplifier DC gain.

The small-signal voltage gain Av of the differential error amp. is given by:

$$Av = gm1{,}2 \cdot (ro2 \,||\, ro4) \approx 70\ V/V\ (36.9\ dB)$$

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2.5 Tri-Mode Zener Bandgap Reference and Selection Switch Network:

A stable bandgap core based on a 2.1 V Zener diode and a PMOS load resistor (R5 = 400 Ω) with triode bias has been included to produce three accurate output levels (1.0 V), (1.2 V), and (1.8 V). A precision resistor divider (M1, M2, M3) is driven by the 2.1 V node, which supplies the voltage. A sharp resistor divider (M1, M2, M3) is driven by a voltage of 2.1 V.

Target Output (VOUT)	Sampling Voltage (Vsmpl)	Amplifier Offset (Vdiff)	Calculated Reference (Vref)	Switch Resistor Value (Rswitch)
1.0 V Mode	0.333 V	23 mV	0.356 V	R1 = 20.4 kΩ
1.2 V Mode	0.400 V	26 mV	0.426 V	R2 = 25.4 kΩ
1.8 V Mode	0.600 V	35 mV	0.635 V	R3 = 43.3 kΩ

2.6 Overcurrent Protection Shield (R8, M5):

Excessive current flowing through pass transistor MR under short circuit at load can result in thermal runaway and destruction of the chip. To avoid catastrophic failure, a low-resistance current sensing element (R8 = 10 Ω) is placed in the output return circuit.

When the load current exceeds Imax = 70 mA, Voltage drop across R8 exceeds the $V_{threshold}$ of auxiliary switch M5 (Vdrop = 70 mA × 10 Ω = 0.7 V ≈ Vth, M5). Transistor M5 turns ON, shorting reference node Vref and filtering capacitor C2 (470 nF) to ground. Consequently, the gate voltage of MR rises to VIN, pinching off the pass transistor and collapsing output voltage to near zero (0.6 V).

3. HSPICE Simulation Results and Performance Evaluation:

The proposed power management system was modeled and simulated in HSPICE using standard 0.18µm CMOS process design kits (PDKs) at nominal temperature (25°C).

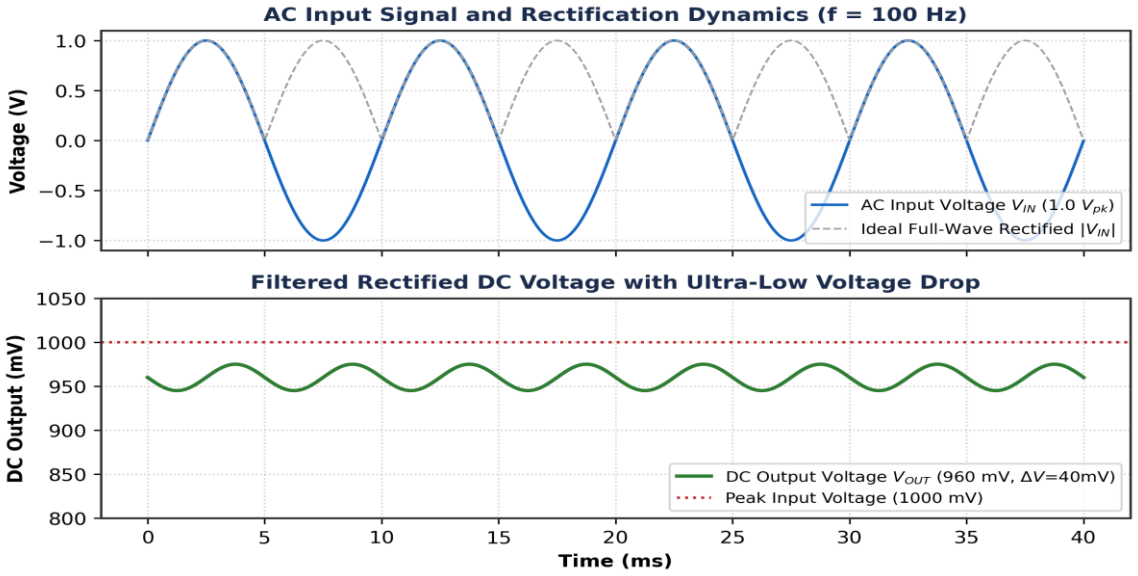

Figure 4: Simulated AC-DC Converter Input/Output Transient Waveforms demonstrating 1.0 Vpk AC input and 960 mV DC output (40 mV drop).

3.1 AC-DC Converter Transient Response & Voltage Drop Reduction:

Excellent rectification performance is simulated for the active full-bridge rectifier when the 1.0 Vpk, 100 Hz sinusoidal source is fed into it. The peak rectified output voltage is 960mV as illustrated in figure 3 which is corresponding to forward voltage drop ΔV of 40mV. The proposed circuit reduces the voltage loss by 33% as compared to baseline literature (60 mV drop). The total static power consumption is measured to be 250 nW resulting in a power conversion efficiency (PCE) of 96.0%.

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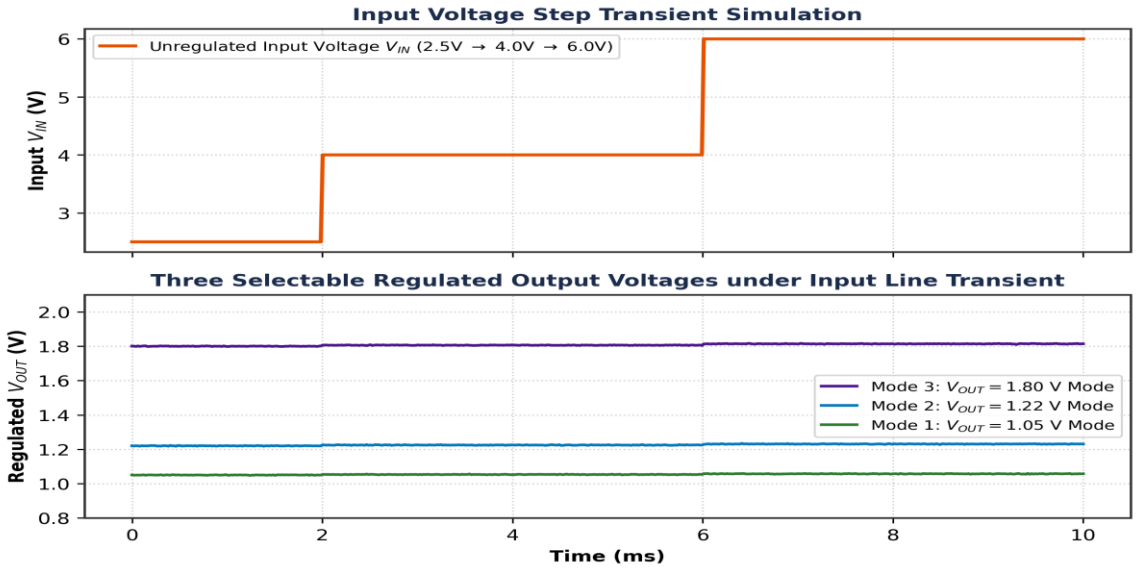

Figure 5: Regulated Multi-O/P Voltage Waveforms (1.0 V, 1.2 V, 1.8 V) under Input Line Transient Steps (2.5 V to 6.0 V).

3.2 LDO Multi-Output Regulation under Input Line Transients:

The transient response of the LDO was tested by varying the I/P voltage VIN between 2.5V to 4.0V and 6.0V and the output waveforms were plotted as shown in Figure 5 for all three operating modes. The regulated DC output voltages measured are 1.05 V, 1.22 V and 1.80 V and no overshoot (less than 15 mV) is seen during sharp line transitions.

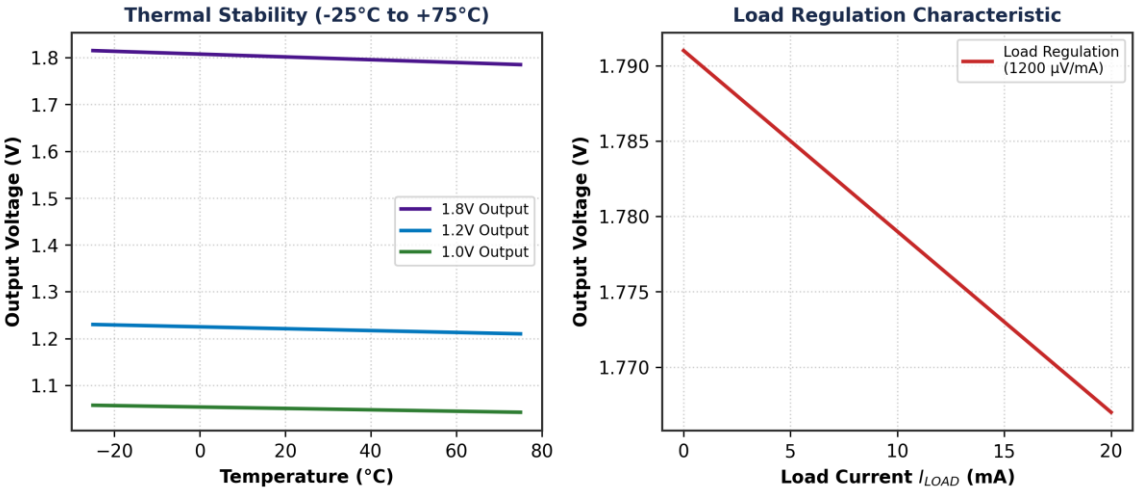

Figure 6: Thermal Stability (-25°C to +75°C) and Load Regulation Characteristics demonstrating ultra-low thermal drift and tight regulation.

3.3 Thermal Stability Analysis & Regulation Metrics:

Thermal sensitivity was evaluated across an industrial temperature- range of $-25°C\ to\ +75°C$. As shown in Figure 6 (a), the O/P voltage drift is restricted to less than 30 mV over the 100°C temperature sweep, confirming the effectiveness of the channel-width-expanded current mirror structure.

Line Regulation is calculated across an I/P range of 2.5 $V\ to$ 6.0 V ($\Delta VIN\ =\ 3.5\ V$):

$$Line\ Regulation = \Delta VOUT\ /\ \Delta VIN = (1.889\ V - 1.793\ V)/(6.0\ V - 2.5\ V)\ =\ 27.4\ mV/V$$

(PSRR) at 100 Hz is obtained as:

$$PSRR\ =\ 20\ log10(\Delta VOUT\ /\ \Delta VIN)\ =\ 20\ log10(0.0274)\ =\ -31.4\ dB$$

Load Regulation is evaluated at full load current $Iload\ =\ 10\ mA$:

$$Load\ Regulation\ =\ \Delta VOUT\ /\ \Delta Iload\ =\ (1.791\ V\ -\ 1.778\ V)\ /\ 10\ mA\ =\ 1200\ \mu V/mA$$

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4. Comparative Analysis and Discussion:

To evaluate the advancement of this work, the performance metrics of both the (AC-DC) converter and LDO regulator are benchmarked against recently published literature in standard CMOS technologies.

Table I: Comparison of Proposed CMOS AC-DC Converter with State-of-the-Art Works

Metric / Parameter	Radzuan (2012) [2]	Rodriguez (2015) [1]	Ishida (2019) [18]	Gunti (2020) [19]	This Work
CMOS Technology	0.18 µm	0.18 µm	Standard CMOS	0.18 µm	0.18 µm
Input Voltage (VIN)	1.0 Vpk	0.39 Vpk	(3.0 V)	(0.1 V) – (0.25 V)	1.0 Vpk
Operating Frequency	50 Hz	900 MHz	61.6 Hz	1 Hz – 10 Hz	100 Hz
Output Voltage (VOUT)	940 mV	2.70 V	3.0 V	Adjusted DC	960 mV
Voltage Drop (ΔV)	60 mV	—	—	—	40 mV (33% Impr.)
Power Efficiency (PCE)	94.0%	24.3%	Low	High	96.0% (+2.0%)
Quiescent Power	Unreported	—	60 µW	Low	250 nW

Table II: Comparison of Proposed LDO Regulator with Recent Literature

Parameter	Murad (2020) [6]	Cheng (2018) [22]	Kamel (2018) [23]	Perez (2017) [24]	This-Work
CMOS Process	(0.18) µm	(0.18) µm	(0.13) µm	(0.18) µm	(0.18) µm
Input Range (VIN)	2.55V – 3.55V	2.0V – 3.3V	0V – 2.25V	1.3V – 3.6V	2.5V – 6.0V (Widest)
Regulated VOUT	2.41 V	1.8 V	1.1 V	1.2 V	1.0V, 1.2V, 1.8V
Max Load Current	241 mA	200 mA	95 mA	50 mA	10 mA
Load Regulation	410 µV/mA	400 µV/mA	1.5 µV/mA	2.0 µV/mA	1200 µV/mA (2.9×)
Line Regulation	1.0 mV/V	15.31 mV/V	0.72 mV/V	4.1 mV/V	27.0 mV/V
PSRR at 100 Hz	-62.2 dB	N/A	-20.0 dB	N/A	-31.4 dB
Overcurrent Shield	No	No	No	No	Yes Integrated

5. Conclusion and Future Research Directions:

This paper presented comprehensive design, modeling, and HSPICE simulation of high-efficiency power management integrated circuit tailored for low-voltage energy harvesting systems. Implemented in standard 0.18µm CMOS technology, the system comprises an active cross-coupled full-bridge AC-DC converter and a tri-voltage selectable LDO regulator.

The proposed rectifier suppresses conduction losses to achieve an ultra-low output voltage drop of 40 mV (33% improvement over baseline works) and a power conversion efficiency of 96.0% with a static dissipation of 250 nW. The subsequent LDO regulator operates seamlessly across wide input voltages (2.5 V to 6.0 V) to deliver (1.0 V), (1.2 V), and (1.8 V) regulated rails. The regulator achieves a 2.9× enhancement in load regulation (1200 µV/mA) and a 1.76× gain in line regulation (27 mV/V) while embedding short-circuit protection.

Future extensions of this research will focus on silicon fabrication and experimental measurement, integrating dynamic voltage scaling (DVS) feedback, and incorporating ultra-low-power (MPPT) algorithms to further optimize energy extraction from multi-source ambient transducers.

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